Computer architecture

Homework week 7 - BONUS

Instructions

Submit by e-mail to the lecturer, as a PDF document with your name and student ID near the beginning. You must work on this alone. Use the English language. Deadline: Oct 28th, 23:59.

The grade of this assignment can be used to replace a grade of another assignment.

Question 1 - DDR (5pt)

1) search on the internet for 3 DDR3 memory modules that match the following constraints:

   - they must be produced by different manufacturers;
   - in 2012;
   - operating at the same frequency.

   For each module, provide the reference name and a link to the corresponding documentation.

2) For each module, determine the DDR memory timings that constrain the access latency and bandwidth, as discovered in the homework week 4+5.

3) For each module, termine quantitatively the minimum read latency (in seconds) and the maximum read bandwidth (in bytes per second).

4) Discuss which one is "better". If available, take the price and capacity of the module into consideration in your argument.

Question 2 - Caches (5pt)

1) Describe the difference between write-back, write-through and write-around caching policies in your own words. If possible, make diagrams to explain.

2) A processor makes 12344 loads and 6379 stores to a write-through cache. The read hit rate is 83%, the write hit rate is 39%. Determine the number of requests sent by the cache to the next memory level.