Computer architecture

Homework week 4

Instructions

Submit by e-mail to the lecturer, as a PDF document with your name and student ID near the beginning. You can work in groups of 2; however, use different groups than week 2 and 3. Use the English language. Deadline: Sept 30th, 23:59.

Answers to bonus questions are counted only if you get at least half the points to each previous question.

Question 1 (5pt)

Search and explain the following terms from the DDR protocol in your own words: tCL, tRCD, tRP, tRAS. Provide the units. If it helps, provide a diagram of how a memory request is handled. Do not use Wikipedia as the primary source.

Question 2 (5pt)

There are two sets of DDR timings in the MGSim configuration file provided with assignment series 1&2a (`minisim.ini`): one for MT41J128M8 and one for Kingston HyperX. You can find them by searching for the words "DDR" inside the file in a text editor. For both configurations, estimate quantitatively the minimum *read* latencies to an individual memory cell from the perspective of the memory controller, considering separately the case where the proper row is already precharged, and the case where another row is already precharged.

> **Hint**
>
> For both question 1 and 2: there is some useful documentation to be found as code comments next to DDR-related stuff in the MGSim sources. Also, to estimate delays the simulation code itself can help.

Question 3 (bonus: 2pt)

Define also tCWL, tCCD and tWR.

Question 4 (bonus: 2pt)

For both configurations from question 2, estimate the minimum *write* latency on both row hit and misses.