Computer architecture

Homework week 2

Instructions

Submit by e-mail to the lecturer, as a PDF document with your name and student ID near the beginning. You can work in groups of 2; however, use different groups than week 1. Use the English language. Deadline: Sept 16th, 23:59.

Question 1

Explain why IPC and CPI are not simply inverse of each other. Use examples.

Question 2

Suppose a 15% reduction in voltage results in a 15% reduction in frequency in a processor chip. What is the impact on dynamic power?

Question 3

Define the terms “fallacy” and “pitfalls” in your own words. Provide examples.

Question 4

In the processor diagram built during the lecture, identify all the individual data buffers (ie decompose the latches), name them and describe textually what is the purpose of the data they hold. For each buffer, also list all the other components/circuits that have access to this buffer.

Question 5

The MGSim core uses a 6-stage RISC pipeline (Fetch, Decode, Read, Execute, Memory, Writeback). At a given CMOS technology size, its L1 cache has an access time of 0,7ns. How does this constrain the maximum frequency of the core?

Question 6

Increasing the L1 cache size increases the access time to 1,4ns. To preserve the cycle time, another memory stage is added to the pipeline. How does this affect the startup time and half-performance vector length?